REMARKS

This communication is a full and timely response to the aforementioned final Office Action dated July 15, 2009 and Advisory Action dated November 25, 2009. By this communication, claims 11-14 and 20 are amended, and claims 21-26 are cancelled. Claims 15-19 are not amended and remain in the application. Thus, claims 11-26 are pending in the application. Claims 11-13 are independent.

Reconsideration of the application and withdrawal of the rejections of the claims are respectfully requested in view of the foregoing amendments and the following remarks.

I. Rejections Under 35 U.S.C. § 103

Claims 11-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 6,617,678, hereinafter "Yamazaki") in view of Abe et al. (U.S. Patent No. 6,205,636, hereinafter "Abe").

Without acquiescing to this rejection, independent claims 11-13 have each been amended to emphasize distinctions between the claimed invention and the applied references. Applicants respectfully submit that the claimed invention is patentable over the applied references for at least the following reasons.

Claim 11 recites a design support apparatus for supporting wiring design for bond wires that connect a semiconductor chip and an interposer. The apparatus of claim 11 comprises an input control unit receiving input data including dimensions of a semiconductor chip and an interposer, and bond wire coordinate information containing arrangement positions of bond wires for connecting the semiconductor chip to the interposer.

The apparatus of claim 11 also comprises a creating unit that creates simulated design data that simulates, based on the input data, an occurrence of deviation in an arrangement position of the semiconductor chip on the interposer, and an occurrence of deviation in bond wire connection terminal positions of the interposer based on the arrangement positions of the bond wires contained in the input data and the simulated deviation in the arrangement position of the semiconductor chip on the interposer.

In addition, the apparatus of claim 11 comprises an analyzing unit that analyzes, based on the simulated design data, deficiencies in manufacturing of semiconductor devices due to the deviation in the arrangement position of the semiconductor chip on the interposer and the deviation in the bond wire connection terminal positions of the interposer, and outputs analysis results that are used to design a semiconductor package based on the input data and the manufacturing deficiencies.

Accordingly, the creating unit in the apparatus of claim 11 creates simulated design data that simulates (1) an occurrence of deviation in an arrangement position of the semiconductor chip on the interposer. In addition, the creating unit creates the simulated design data that simulates (2) an occurrence of deviation in bond wire connection terminal positions of the interposer based on the arrangement positions of the bond wires contained in the input data and the simulated deviation in the arrangement position of the semiconductor chip on the interposer. Therefore, the simulation of the occurrence of the deviation in bond wire connection terminals is predicated on the simulation of the arrangement position of the semiconductor chip on the interposer. Furthermore, claim 11 recites that the creating unit creates the simulated design data prior to arrangement of the semiconductor chip on the interposer.

The applied references do not disclose or suggest all the recited features of claim 11, for at least the following reasons.

Yamazaki discloses a technique of mounting laminated semiconductor chips 3 onto a substrate 2 and connecting relay terminals 5 of the substrate 2 to terminal pads 19 of the chips 3 via wirings 6 (see Figures 1 and 3). The technique of Yamazaki is an extension of the prior art technique illustrated in Figure 7 of Yamazaki. In the prior art technique illustrated in Figure 7, Yamazaki discloses that the center C of the semiconductor chip 3 is matched to the center X of the substrate 2 and the center Z of the device package (see Column1, lines 44-48). Each wiring 106 is based on a predefined wiring rule (design rule) (see Column 2, lines 64-67). Due to different shapes of chips 103 and the predefined arrangement of via terminals 105 relative to the pads 107 of the chips 103, a problem can occur in the wiring state in complying with the predefined wiring rule. For instance, as illustrated in Figure 7,

the wiring pattern on the substrate 102 may include a mixture of wirings 106 arranged at coarse intervals (shown by "L" in Figure 7) and/or a mixture of wirings 106 arranged at dense intervals (shown by "H" in Figure 7) (see Column 2, lines 21-37). This difficulty with the wiring pattern results because of required adherence to the predefined wiring rule.

The embodiments of Yamazaki disclosed in Figures 1 and 3, for example, propose a different technique of mounting the semiconductor chips 3 so that adherence with the predetermined wiring rule 3 can be maintained. With respect to the embodiment illustrated in Figure 1, Yamazaki discloses that the center C of the semiconductor chip 3 is offset by a distance A from the center X of the substrate 2, the center Y of the relay terminals 5 of the substrate 2, and the center Z of the device package. Accordingly, prior to actually mounting the semiconductor chip 3 on the substrate 2, the center X of the substrate 2, the center Y of the relay terminals 5 and the center Z of the device package must each be aligned so that the center C of the semiconductor chip 3 can thereafter be aligned (see Column 7, lines 5-24).

Yamazaki discloses that the center C of the semiconductor chip 3 is offset by distance A to avoid the coarse ("L" in Figure 7) and/or dense ("H" in Figure 7) wiring intervals associated with the prior art technique, and still comply with the predetermined wiring rule (see Column 7, lines 46-56). In particular, Yamazaki discloses that by offsetting the center C of the semiconductor chip 3 by distance A, relative to the centers X, Y, Z of the substrate 2, relay terminals 5 and device package, so that the wiring scheme will comply with the predetermined wiring rule (see Column 7, lines 57-67). Figure 3 of Yamazaki illustrates another embodiment in which, in addition to offsetting the center C of the semiconductor chip 3 by distance A, the orientation of the semiconductor chip 3 is rotated by angle Θ (see Column 10, lines 44-55). Otherwise, the embodiment of Figure 3 is similar to the embodiment of Figure 1 in that the arrangement of the relay terminals 5 and the arrangement of the substrate 2 is fixed due to the alignment of centers X, Y, Z.

Once the offset position of the semiconductor chip 3 is determined according to the embodiments of either Figure 1 or Figure 3, Yamazaki discloses that the semiconductor chip 3 is then physically mounted to the substrate 2. The operation of mounting the semiconductor chip 3 to the substrate 2 is performed because the

orientation of the semiconductor chip 2 is performed to allow adherence to the predetermined wiring rule. Assuming the center C of the semiconductor chip 3 is offset to a correct position, adherence to the predetermined wiring rule is enabled because the positions of the relay terminals 5 have been fixed, thereby allowing placement of the wirings 6 to adhere to the predetermined wiring rule (see Column 8, lines 35-48 and 59-65).

Accordingly, Yamazaki discloses that after the semiconductor chip 3 has been mounted to the substrate 2, the positions of the wirings 6 are completed so that the wirings adhere to the predetermined wiring rule.

Therefore, in contrast to claim 11, Yamazaki does not disclose or suggest that simulated design data is created to simulate (1) an occurrence of deviation in an arrangement position of the semiconductor chip on the interposer, and (2) an occurrence of deviation in bond wire connection terminal positions of the interposer based on the arrangement positions of the bond wires contained in the input data and the simulated deviation in the arrangement position of the semiconductor chip on the interposer.

In particular, Yamazaki does not disclose or suggest that an occurrence of deviation in bond wire connection terminal positions of the substrate 2 is simulated based on a simulated deviation in the arrangement position of the semiconductor chip 3, because the position of the substrate 2 and the positions of the relay terminals 5 of the substrate 2 are fixed prior to any offsetting of the semiconductor chip 3. Yamazaki explicitly requires that the center X of the substrate 2, the center Y of the relay terminals 5, and the center Z of the device package be "calculated beforehand" prior to the offset arrangement of the semiconductor chip 3 on the substrate 2 (see Column 7, lines 13-19) (emphasis added).

Accordingly, in contrast to claim 11, Yamazaki does not disclose or suggest that simulated design data is created to simulate (1) an occurrence of deviation in an arrangement position of the semiconductor chip on the interposer, and (2) an occurrence of deviation in bond wire connection terminal positions of the interposer based on the arrangement positions of the bond wires contained in the input data and the simulated deviation in the arrangement position of the semiconductor chip on the interposer.

Furthermore, Yamazaki does not disclose or suggest that the simulated design data including features (1) and (2) above is created prior to arrangement of the semiconductor chip on the interposer. Yamazaki discloses an opposite technique, in that wirings 106 are fitted between relay terminals 5, whose positions have been fixed, and terminal pads 14, whose positions have also been fixed because the semiconductor chip 3 has been mounted to the substrate 2.

Therefore, Applicants respectfully submit that Yamazaki does not disclose or suggest the creating unit as recited in claim 11. By failing to disclose or suggest the creating unit, Yamazaki cannot disclose or suggest the analyzing unit of claim 11 which analyzes the simulated design data created by the creating unit.

Abe also does not disclose or suggest the features of the creating unit and analyzing unit as recited in claim 11.

Abe discloses an apparatus for automatically assembling a product, in which the apparatus includes an image recognition unit and a mechanical assembly unit. With reference to Figure 1, the image taking section 7 (which includes a camera 8, a zoom optical system 9, and a zoom motor 10), the image recognition section 11, the CPU 18, the memory device 19, the monitor display 20, the key entry section 21 and the mechanism control section 17 constitute the image recognition unit (see Column 4, lines 26-32). The objective of Abe is to align the image recognition unit with the actual mechanical operating parameters of the mechanical assembly unit, so that the product can be assembled automatically.

To align the image recognition unit, a reference mark having known dimensions is first pictured through the camera 8, to compile a data table of measured pixel rates and offset values (pictured location versus actual location) in order to align the image recognition unit properly (see Column 5, lines 1-6, and Column 6, lines 34-53). This initial registration procedure intends to ensure that when the product is automatically assembled, the positions recognized by the image recognition unit will match the actual positions. In particular, with reference to Figure 6, a known diameter of a jig is measured through the camera 8 to determine the recognition offset (Cx, Cy) of the camera 8, relative to the known position and diameter of the jig. This calibration process produces the recognition offset Cx, Cy, a zoom magnification index n, and a pixel rate Px, Py (see Column 6, lines 34-54).

The pixel rate is a mathematical coefficient for converting the dimension of an actual object to the representation of the object in an image taken by the camera 8. In other words, the pixel rate is a conversion factor identifying an actual position size relative to the size of an object represented in an image taken by the camera 8 (see Column 6, lines 54-63). Once the values of the pixel rate Px, Py and recognition offset Cx, Cy are determined relative to the actual position of the point of measurement, the values are fixed for the assembly process (see Column 6, line 64 to Column 7, line 6), provided that the zoom magnification index, which is represented by the zoom coordinate Z, is kept constant. The zoom magnification index is a numerical value representing the degree of zoom of the camera 8 relative to a number of revolutions of a zoom motor 10 for changing the zoom focus of the camera 8 (see Column 7, lines 1-14).

Abe thus discloses a calibration technique for calibrating actual positions with positions measured by a camera 8, so that automatic assembly can be completed based on positions observed by the camera 8 during assembly. Therefore, Abe merely discloses a process by which imaged values are calibrated against actual values.

However, similar to Yamazaki, Abe does not disclose or suggest does not disclose or suggest that simulated design data is created to simulate (1) an occurrence of deviation in an arrangement position of the semiconductor chip on the interposer, and (2) an occurrence of deviation in bond wire connection terminal positions of the interposer based on the arrangement positions of the bond wires contained in the input data and the simulated deviation in the arrangement position of the semiconductor chip on the interposer. Furthermore, similar to Yamazaki, Abe does not disclose or suggest that the simulated design data including features (1) and (2) above is created prior to arrangement of the semiconductor chip on the interposer. On the contrary, Abe discloses an opposite technique of calibrating measured values against actual, measured values.

Accordingly, similar to Yamazaki, Abe also does not disclose or suggest the features of the creating unit and analyzing unit as recited in claim 11.

Therefore, Applicants respectfully submit that claim 11 is patentable over Yamazaki and Abe, since Yamazaki and Abe, either individually or in combination,

fail to disclose or suggest all the recited features of the claimed invention. Furthermore, in view of the distinctions discussed above, Applicants respectfully submit that one skilled in the art would not have reason or been motivated to modify Yamazaki and Abe in an attempt to arrive at the features of claim 11.

Although of different scope, claims 12 and 13 recite features similar to those discussed above which are not disclosed or suggested by the combination of Yamazaki and Abe. Therefore, Applicants respectfully submit that claims 12 and 13 are patentable over Yamazaki and Abe for reasons similar to those presented above with respect to claim 11.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that claims 11-13, as well as claims 14-26 which depend therefrom, are patentable over the applied references.

Dependent claims 14-26 recite further distinguishing features over the applied references and are also patentable by virtue of depending from claims 11-13. The foregoing explanation of the patentability of claims 11-13 is sufficiently clear such that it is believed to be unnecessary to separately demonstrate the additional patentable features of the dependent claims at this time. However, Applicants reserve the right to do so should it become appropriate.

II. Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. Accordingly, a favorable examination and consideration of the instant application are respectfully requested.

If, after reviewing this Response, the Examiner believes there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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